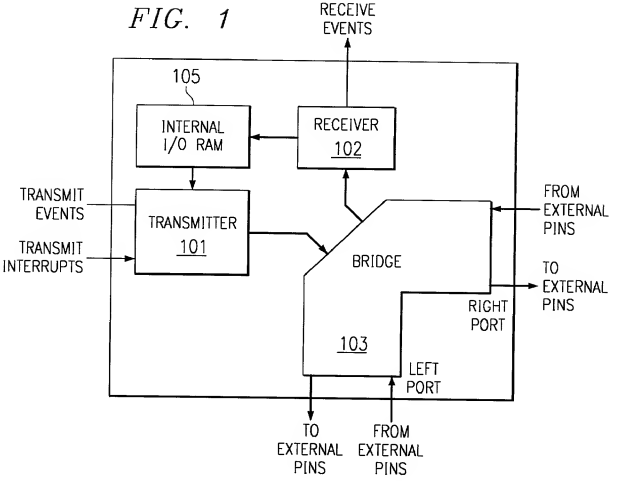
FIG. 1


RECEIVE EVENTS
105
INTERNAL I/O RAM
RECEIVER 102
TRANSMIT EVENTS
TRANSMITTER 101
TRANSMIT INTERRUPTS
BRIDGE
FROM EXTERNAL PINS
TO EXTERNAL PINS
RIGHT PORT
103
LEFT PORT
TO EXTERNAL PINS
FROM EXTERNAL PINS

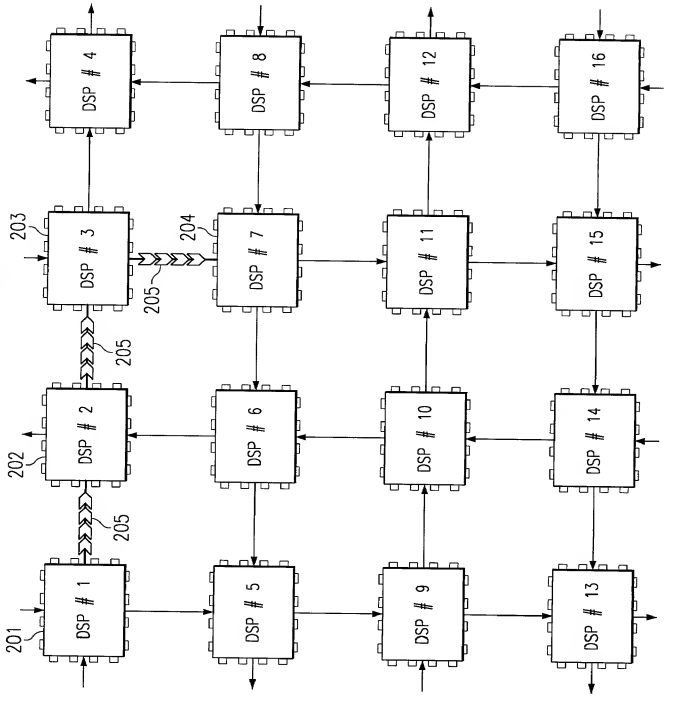

DSP # 1
DSP # 2
DSP # 3
DSP # 4
DSP # 5
DSP # 6
DSP # 7
DSP # 8
DSP # 9
DSP # 10
DSP # 11
DSP # 12
DSP # 13
DSP # 14
DSP # 15
DSP # 16
201
202
203
204
205
205
205

FIG. 2

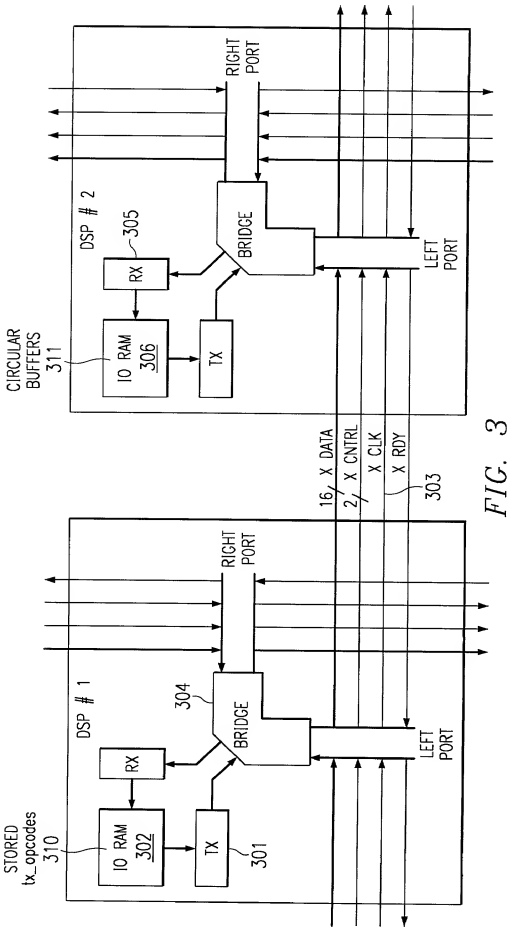

STORED
tx_opcodes
310
IO RAM
302
TX
301
RX
DSP # 1
304
BRIDGE
RIGHT
PORT
LEFT
PORT
16 X DATA
2 X CNTRL
X CLK
X RDY
303
CIRCULAR
BUFFERS
311
IO RAM
306
TX
RX
305
DSP # 2
BRIDGE
RIGHT
PORT
LEFT
PORT

FIG. 3

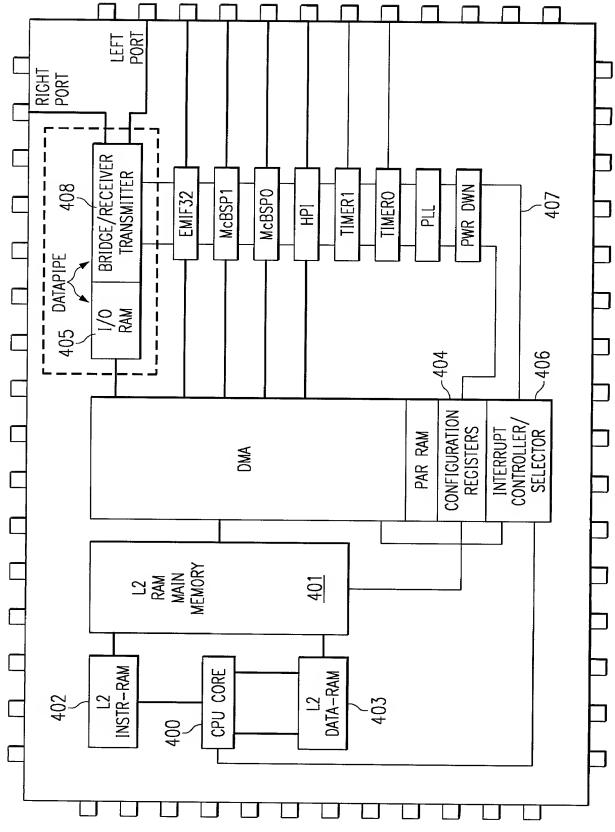

RIGHT PORT
LEFT PORT
DATAPIPE
408
405
I/O RAM
BRIDGE/RECEIVER TRANSMITTER
EMIF32
McBSP1
McBSP0
HPI
TIMER1
TIMER0
PLL
PWR DWN
407
DMA
PAR RAM
CONFIGURATION REGISTERS
INTERRUPT CONTROLLER/ SELECTOR
404
406
L2 RAM MAIN MEMORY
401
402
L2 INSTR-RAM
400
CPU CORE
L2 DATA-RAM
403

FIG. 4

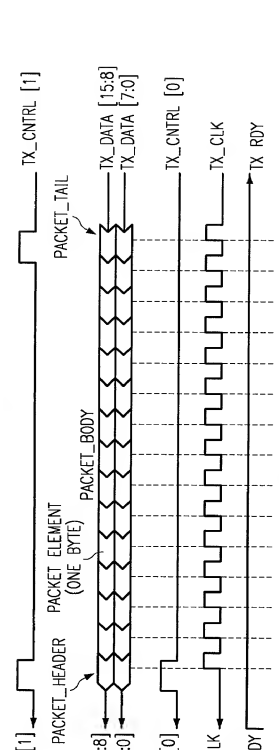

RX_CNTRL [1]
PACKET_HEADER
PACKET ELEMENT (ONE BYTE)
PACKET_BODY
PACKET_TAIL
RX_DATA [15:8]
RX_DATA [7:0]
RX_CNTRL [0]
RX CLK
RX RDY
TX_CNTRL [1]
TX_DATA [15:8]
TX_DATA [7:0]
TX_CNTRL [0]
TX_CLK
TX RDY

FIG. 5

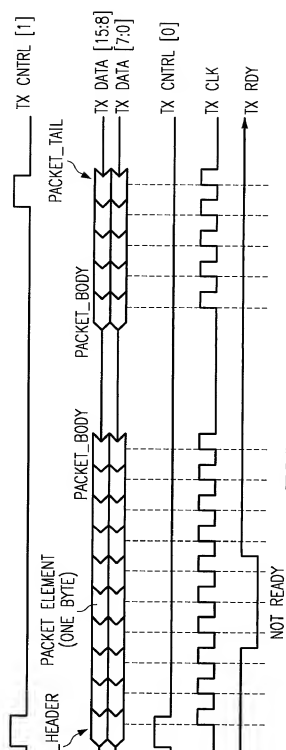

RX CNTRL [1]
PACKET_HEADER
PACKET ELEMENT (ONE BYTE)
PACKET_BODY
PACKET_TAIL
RX DATA [15:8]
RX DATA [7:0]
RX CNTRL [0]
RX CLK
RX RDY
NOT READY
TX CNTRL [1]
TX DATA [15:8]
TX DATA [7:0]
TX CNTRL [0]
TX CLK
TX RDY

FIG. 6

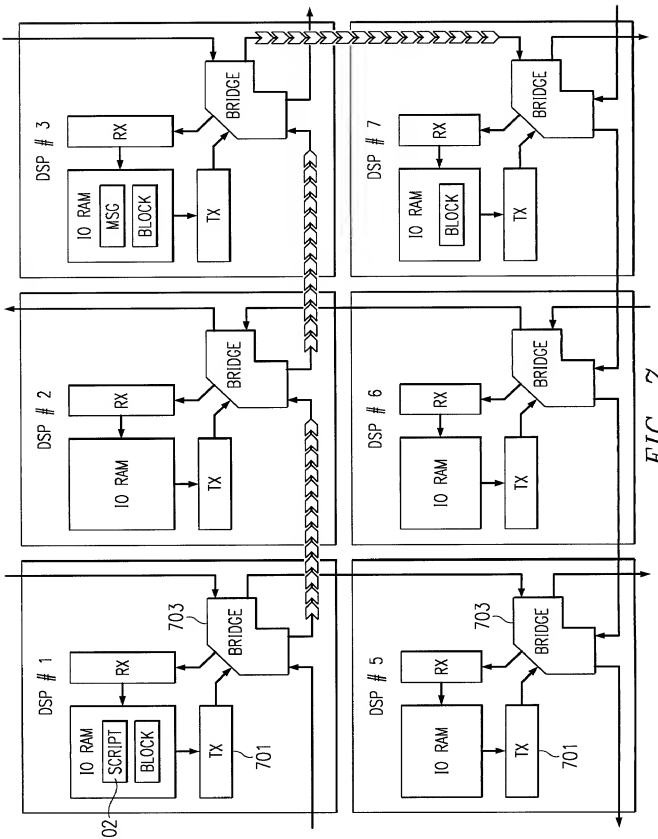

DSP # 1
IO RAM
SCRIPT
BLOCK
RX
TX
BRIDGE
702
701
703
DSP # 2
IO RAM
RX
TX
BRIDGE
DSP # 3
IO RAM
MSG
BLOCK
RX
TX
BRIDGE
DSP # 5
IO RAM
RX
TX
BRIDGE
703
701
DSP # 6
IO RAM
RX
TX
BRIDGE
DSP # 7
IO RAM
BLOCK
RX
TX
BRIDGE

FIG. 7

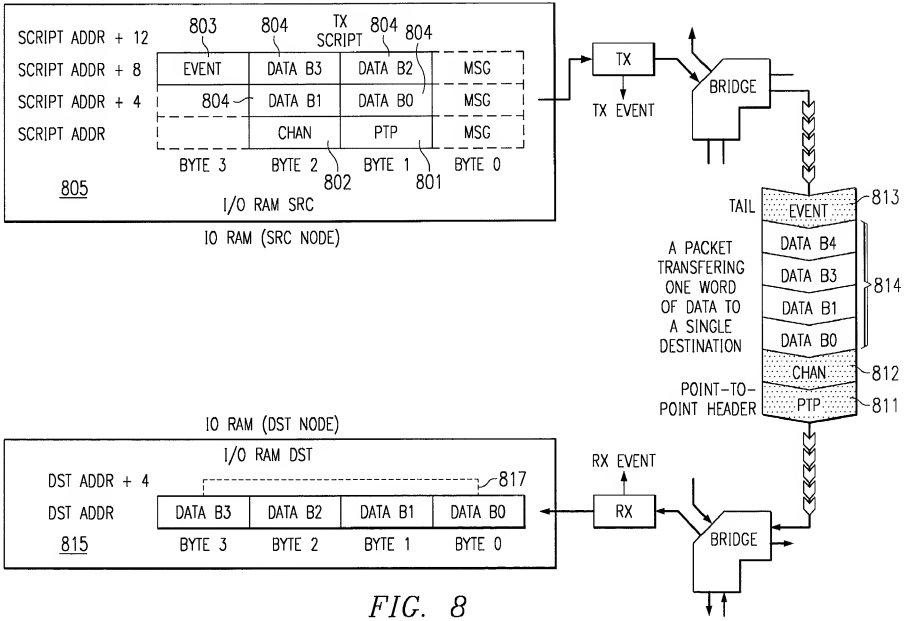

SCRIPT ADDR + 12
SCRIPT ADDR + 8
SCRIPT ADDR + 4
SCRIPT ADDR
803
804
TX SCRIPT
804
804
EVENT
DATA B3
DATA B2
MSG
804
DATA B1
DATA B0
MSG
CHAN
PTP
MSG
BYTE 3
BYTE 2
BYTE 1
BYTE 0
802
801
805
I/O RAM SRC
IO RAM (SRC NODE)
TX
TX EVENT
BRIDGE
TAIL
EVENT
813
A PACKET TRANSFERING ONE WORD OF DATA TO A SINGLE DESTINATION
DATA B4
DATA B3
DATA B1
DATA B0
814
CHAN
812
POINT-TO-POINT HEADER
PTP
811
IO RAM (DST NODE)
I/O RAM DST
DST ADDR + 4
DST ADDR
817
DATA B3
DATA B2
DATA B1
DATA B0
BYTE 3
BYTE 2
BYTE 1
BYTE 0
815
RX EVENT
RX
BRIDGE

FIG. 8

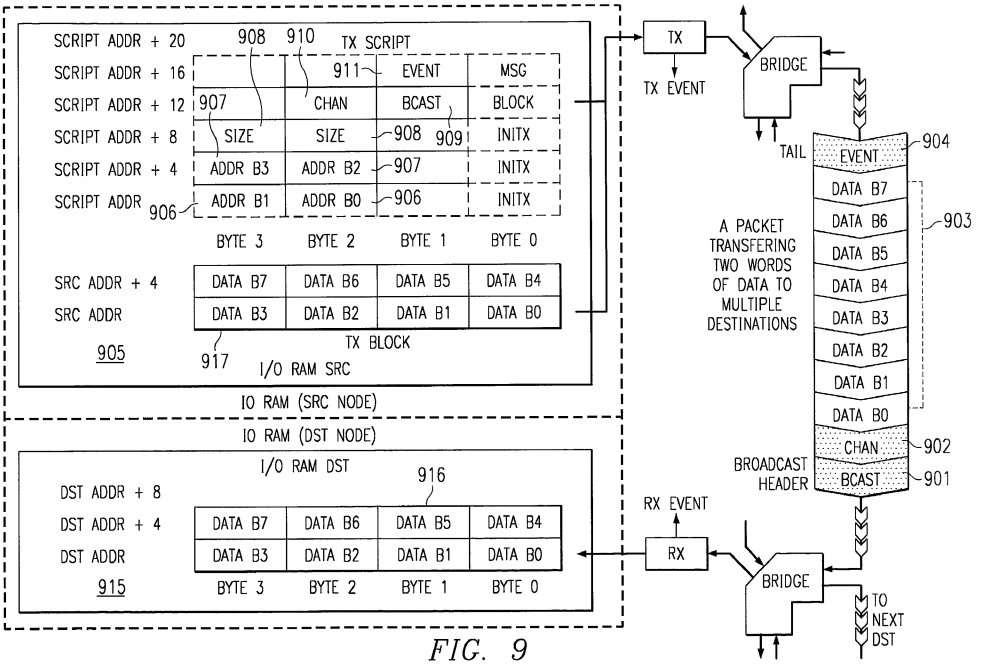

SCRIPT ADDR + 20
SCRIPT ADDR + 16
SCRIPT ADDR + 12
SCRIPT ADDR + 8
SCRIPT ADDR + 4
SCRIPT ADDR
906
908
910
911
907
909
TX SCRIPT
EVENT
MSG
CHAN
BCAST
BLOCK
SIZE
SIZE
INITX
ADDR B3
ADDR B2
INITX
ADDR B1
ADDR B0
INITX
BYTE 3
BYTE 2
BYTE 1
BYTE 0
SRC ADDR + 4
SRC ADDR
DATA B7
DATA B6
DATA B5
DATA B4
DATA B3
DATA B2
DATA B1
DATA B0
TX BLOCK
905
917
I/O RAM SRC
IO RAM (SRC NODE)
IO RAM (DST NODE)
I/O RAM DST
916
DST ADDR + 8
DST ADDR + 4
DST ADDR
915
BYTE 3
BYTE 2
BYTE 1
BYTE 0
TX
TX EVENT
BRIDGE
TAIL
EVENT
904
DATA B7
DATA B6
DATA B5
DATA B4
DATA B3
DATA B2
DATA B1
DATA B0
903
A PACKET TRANSFERING TWO WORDS OF DATA TO MULTIPLE DESTINATIONS
CHAN
902
BROADCAST HEADER
BCAST
901
RX EVENT
RX
BRIDGE
TO NEXT DST

FIG. 9

TOETZO"8ZESU66U

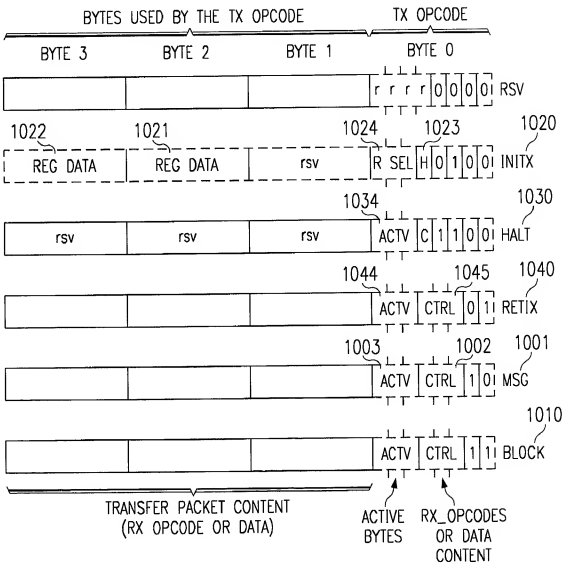


FIG. 10

RESERVED FOR FUTURE USE

INITIALIZE TRANSMITTER REGISTER(S)

HALT EXECUTION OF BATCH OPCODES

RETURN FROM INTERRUPT SCRIPT
TO BATCH SCRIPT

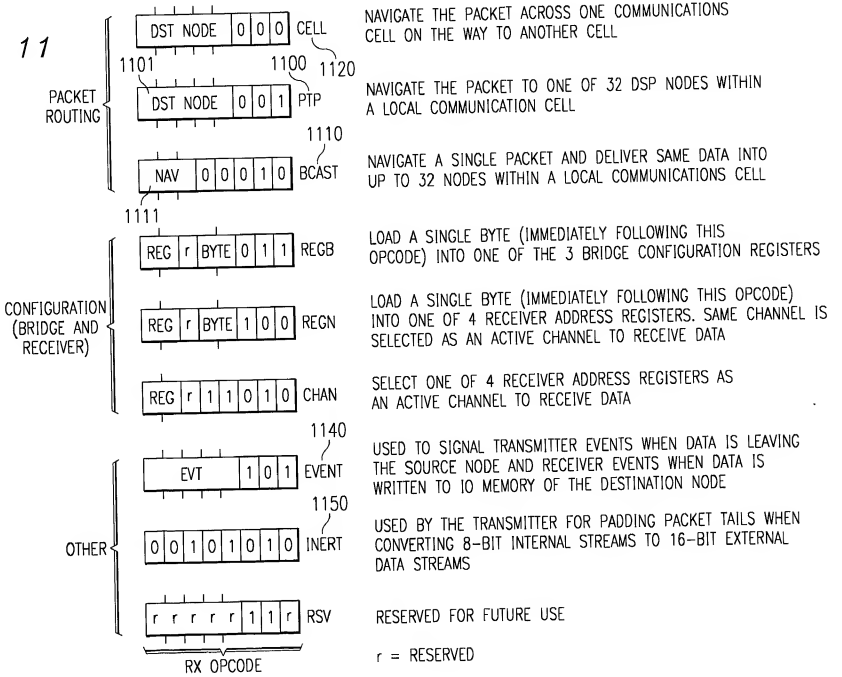
TRANSMIT DATA/RX_OPCODES
EMBEDDED IN TX OPCODE

TRANSMIT A DATA BLOCK LOCATED
ELSEWHERE IN I/O RAM

r = RESERVED

0982078 '8268990

FIG. 11



NAVIGATE THE PACKET ACROSS ONE COMMUNICATIONS CELL ON THE WAY TO ANOTHER CELL

NAVIGATE THE PACKET TO ONE OF 32 DSP NODES WITHIN A LOCAL COMMUNICATION CELL

NAVIGATE A SINGLE PACKET AND DELIVER SAME DATA INTO UP TO 32 NODES WITHIN A LOCAL COMMUNICATIONS CELL

LOAD A SINGLE BYTE (IMMEDIATELY FOLLOWING THIS OPCODE) INTO ONE OF THE 3 BRIDGE CONFIGURATION REGISTERS

LOAD A SINGLE BYTE (IMMEDIATELY FOLLOWING THIS OPCODE) INTO ONE OF 4 RECEIVER ADDRESS REGISTERS. SAME CHANNEL IS SELECTED AS AN ACTIVE CHANNEL TO RECEIVE DATA

SELECT ONE OF 4 RECEIVER ADDRESS REGISTERS AS AN ACTIVE CHANNEL TO RECEIVE DATA

USED TO SIGNAL TRANSMITTER EVENTS WHEN DATA IS LEAVING THE SOURCE NODE AND RECEIVER EVENTS WHEN DATA IS WRITTEN TO IO MEMORY OF THE DESTINATION NODE

USED BY THE TRANSMITTER FOR PADDING PACKET TAILS WHEN CONVERTING 8-BIT INTERNAL STREAMS TO 16-BIT EXTERNAL DATA STREAMS

RESERVED FOR FUTURE USE

r = RESERVED

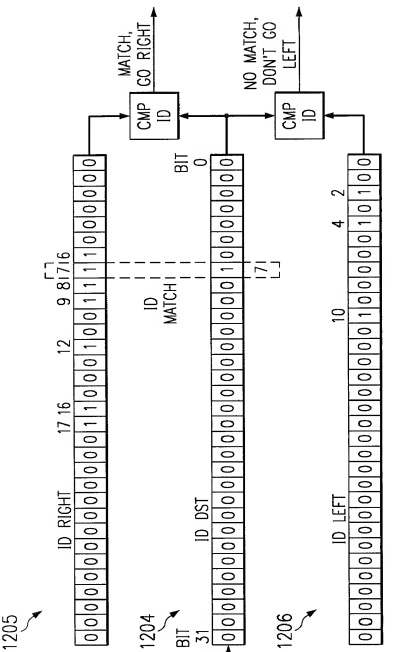

EVENT
DATA
PTP
1201
DST NODE
0 0 1
1202
NODE ADDR
0 0 1 0 1
0 0 1 1 1
CMP ADDR
NO MATCH,
DON'T EXIT INTO
THIS NODE
DECODE
1203
1205
ID RIGHT
17 16
12
9 8
1 7 6
1204
BIT
31
ID DST
ID
MATCH
BIT
0
1 7 1
1206
ID LEFT
10
4
2
CMP
ID
MATCH,
GO RIGHT
CMP
ID
NO MATCH,
DON'T GO
LEFT

FIG. 12

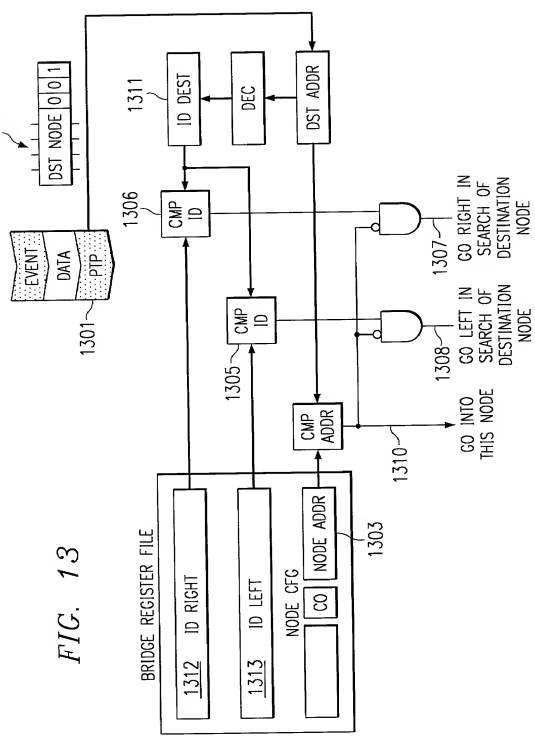

1302
DST NODE 0 0 1
EVENT
DATA
PTP
1301
1311
ID DEST
DEC
DST ADDR
1306
CMP ID
1305
CMP ID
CMP ADDR
1310
1307
GO RIGHT IN SEARCH OF DESTINATION NODE
1308
GO LEFT IN SEARCH OF DESTINATION NODE
GO INTO THIS NODE
BRIDGE REGISTER FILE
1312 ID RIGHT
1313 ID LEFT
NODE CFG
CO
NODE ADDR
1303

FIG. 13

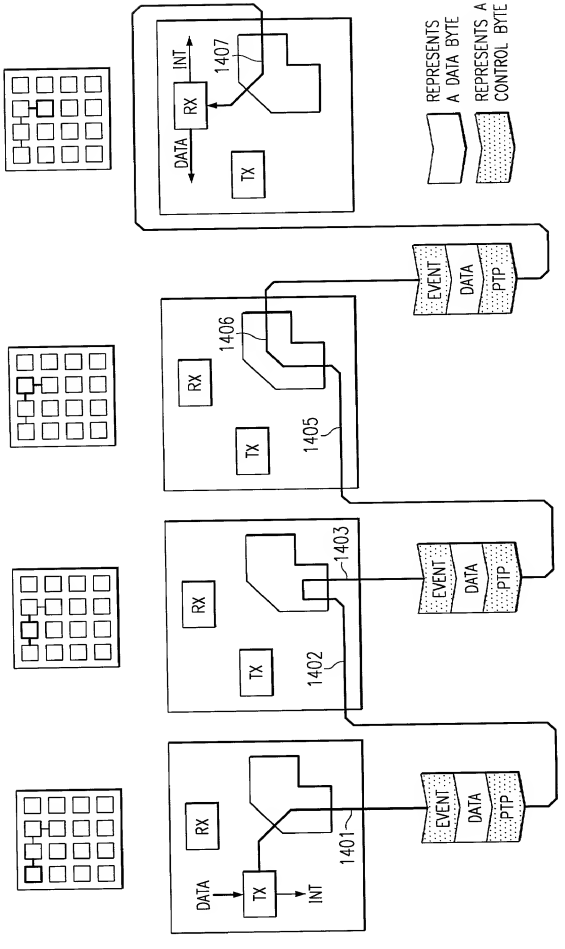
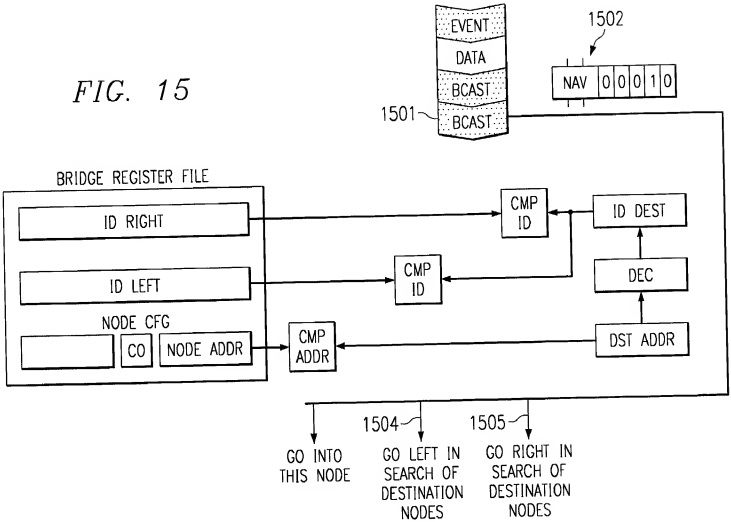

DATA
TX
INT
RX
1401
EVENT
DATA
PTP
TX
RX
1402
1403
EVENT
DATA
PTP
TX
RX
1405
1406
EVENT
DATA
PTP
DATA
TX
RX
INT
1407
REPRESENTS A DATA BYTE
REPRESENTS A CONTROL BYTE

FIG. 14

TOETZU 8ZESU660

FIG. 15



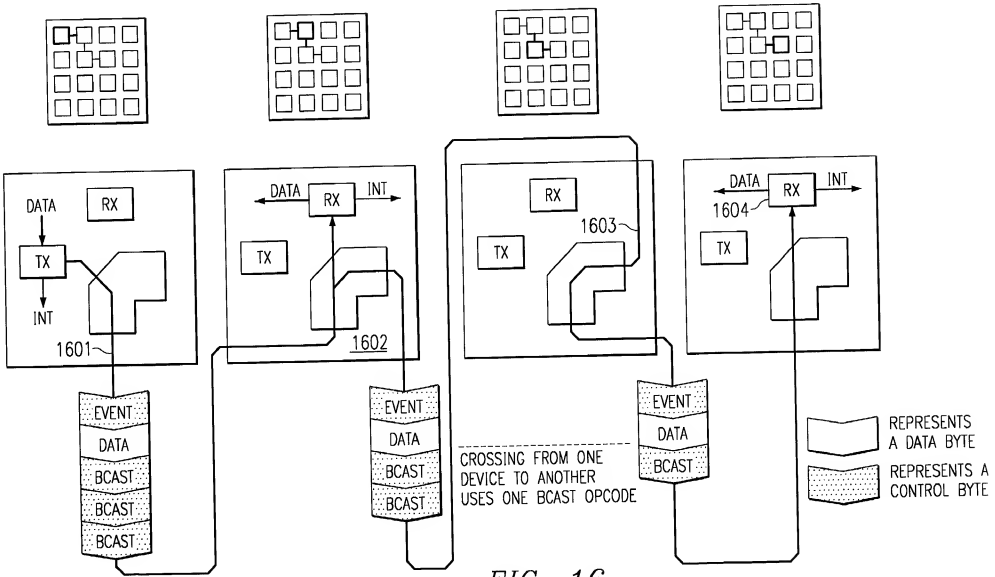
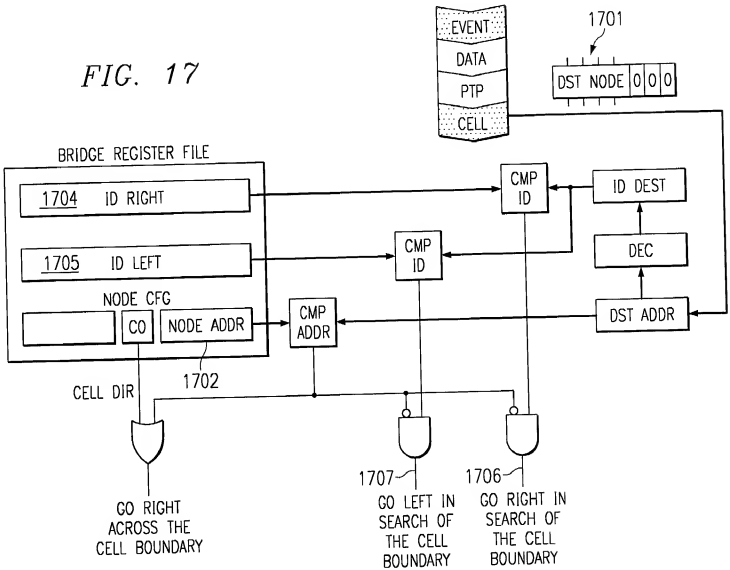

DATA
RX
TX
INT
1601
EVENT
DATA
BCAST
BCAST
BCAST
DATA
RX
INT
TX
1602
EVENT
DATA
BCAST
BCAST
RX
1603
TX
CROSSING FROM ONE
DEVICE TO ANOTHER
USES ONE BCAST OPCODE
EVENT
DATA
BCAST
DATA
RX
INT
1604
TX
REPRESENTS
A DATA BYTE
REPRESENTS A
CONTROL BYTE

FIG. 16

TOETZ0*8ZES0660

FIG. 17



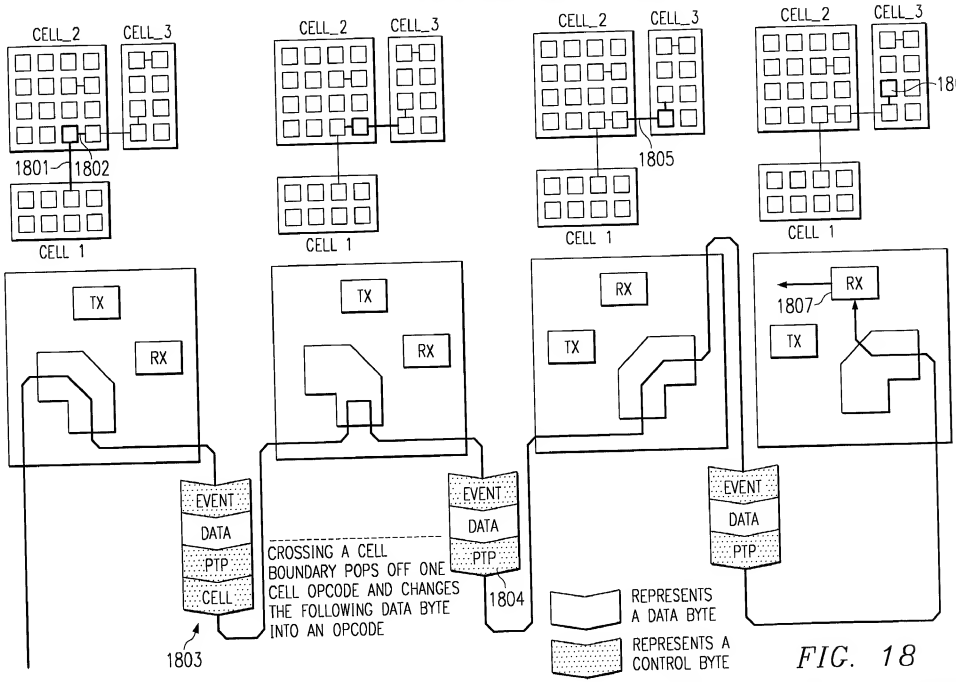

CELL_2
CELL_3
1801
1802
CELL 1
1805
1806
1807
TX
RX
EVENT
DATA
PTP
CELL
1803
1804
CROSSING A CELL BOUNDARY POPS OFF ONE CELL OPCODE AND CHANGES THE FOLLOWING DATA BYTE INTO AN OPCODE
REPRESENTS A DATA BYTE
REPRESENTS A CONTROL BYTE

FIG. 18

TOETZO*8ZES0660

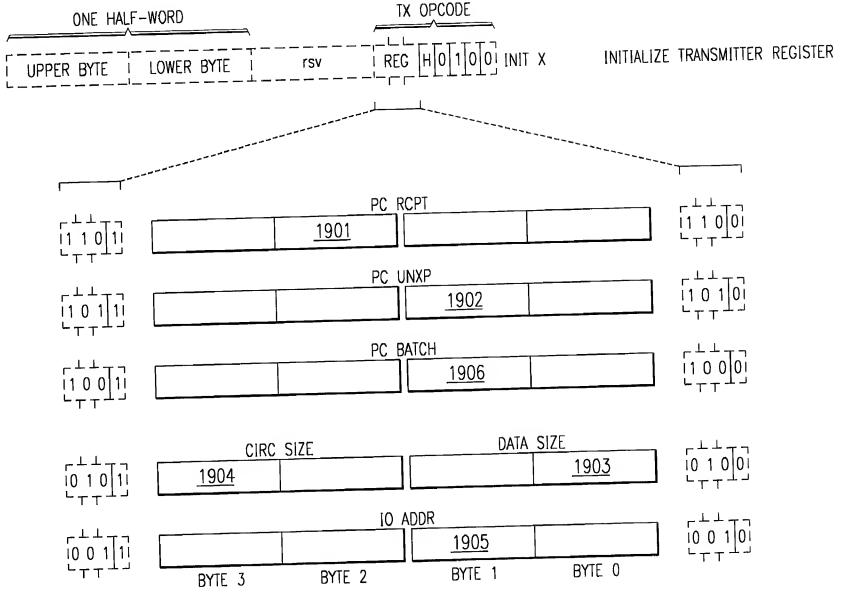
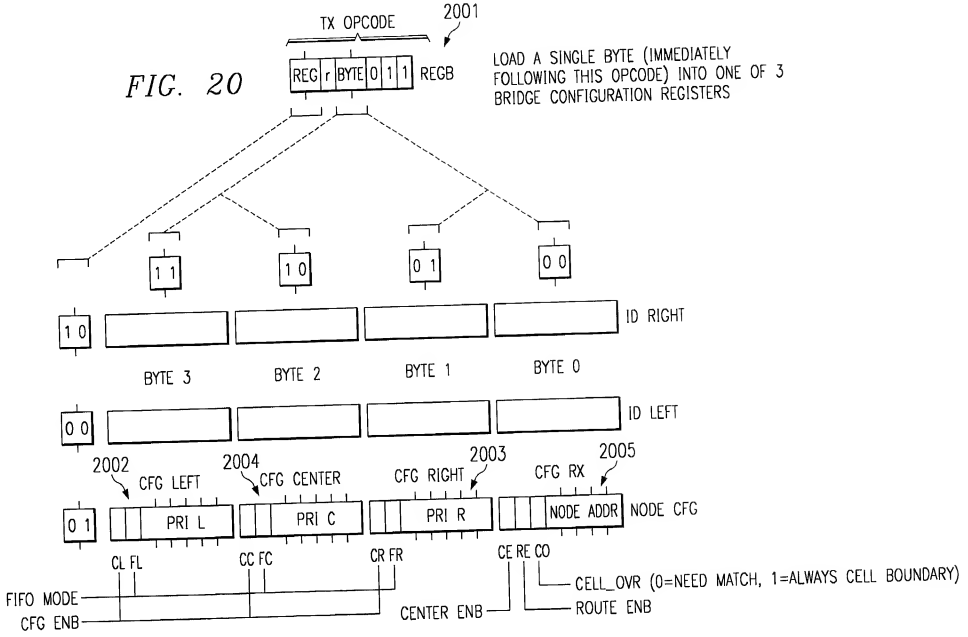


FIG. 19

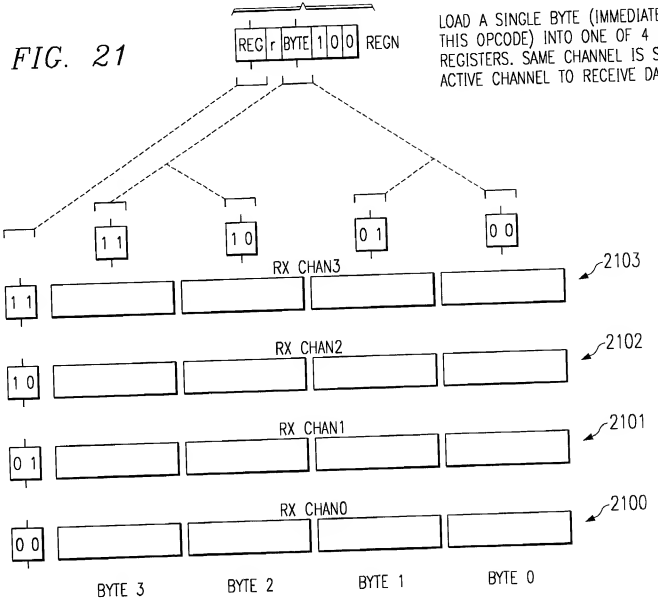
DOCKET# 82650660

FIG. 20



09052729 "07130"

FIG. 21



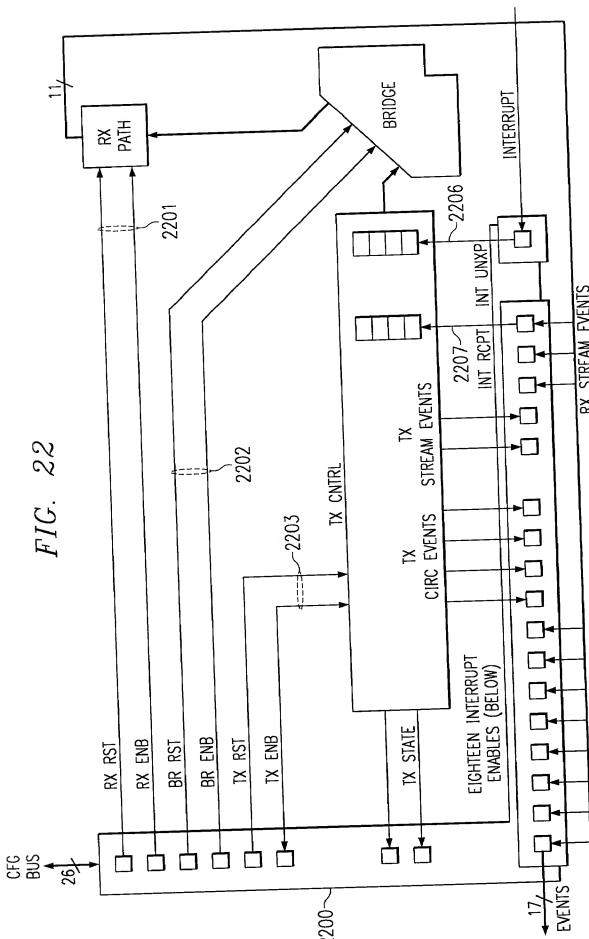

11
RX PATH
BRIDGE
2201
2206
INTERRUPT
INT UNXP
INT RCPT
2207
2205
RX STREAM EVENTS
TX STREAM EVENTS
2202
TX CNTRL
2203
TX CIRC EVENTS
EIGHTEEN INTERRUPT ENABLES (BELOW)
RX CIRC EVENTS
2204
CFG BUS
26
RX RST
RX ENB
BR RST
BR ENB
TX RST
TX ENB
TX STATE
2200
17
EVENTS

FIG. 22

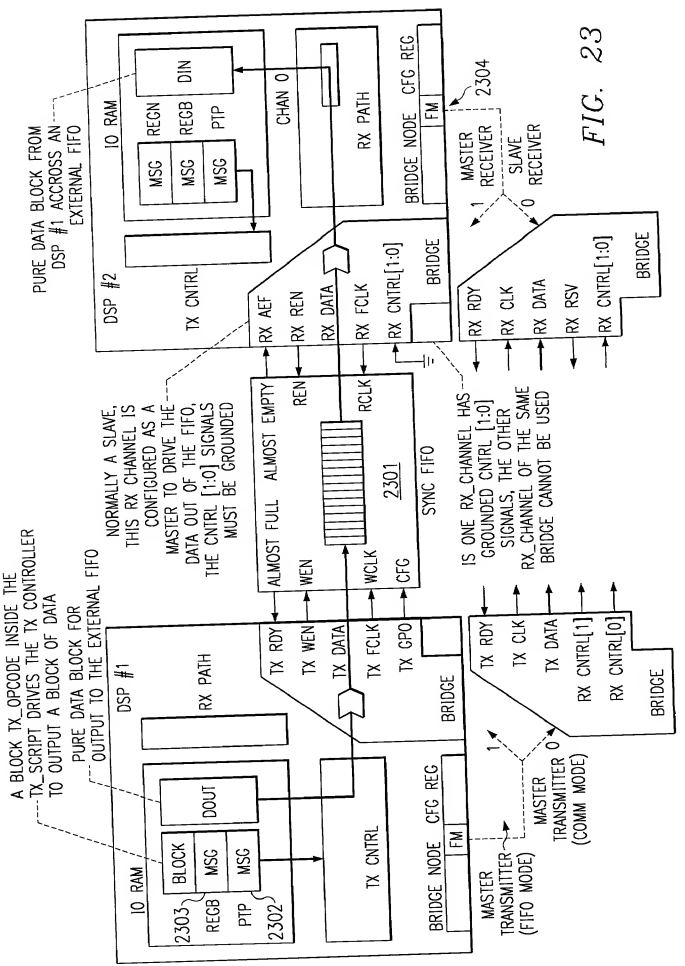

A BLOCK TX_OPCODE INSIDE THE TX_SCRIPT DRIVES THE TX CONTROLLER TO OUTPUT A BLOCK OF DATA
PURE DATA BLOCK FOR OUTPUT TO THE EXTERNAL FIFO
NORMALLY A SLAVE, THIS RX CHANNEL IS CONFIGURED AS A MASTER TO DRIVE THE DATA OUT OF THE FIFO, THE CNTRL [1:0] SIGNALS MUST BE GROUNDED
PURE DATA BLOCK FROM DSP #1 ACCROSS AN EXTERNAL FIFO
IS ONE RX_CHANNEL HAS GROUNDED CNTRL [1:0] SIGNALS, THE OTHER RX_CHANNEL OF THE SAME BRIDGE CANNOT BE USED
DSP #1
IO RAM
BLOCK
DOUT
MSG
MSG
REGB
PTP
2303
2302
TX CNTRL
RX PATH
BRIDGE NODE CFG REG
FM
MASTER TRANSMITTER (FIFO MODE)
MASTER TRANSMITTER (COMM MODE)
1
0
TX RDY
TX WEN
TX DATA
TX FCLK
TX GPO
BRIDGE
ALMOST FULL
ALMOST EMPTY
WEN
REN
WCLK
RCLK
CFG
2301
SYNC FIFO
TX RDY
TX CLK
TX DATA
RX CNTRL[1]
RX CNTRL[0]
BRIDGE
DSP #2
IO RAM
REGN
REGB
PTP
DIN
MSG
MSG
MSG
TX CNTRL
CHAN 0
RX PATH
BRIDGE NODE CFG REG
FM
RX AEF
RX REN
RX DATA
RX FCLK
RX CNTRL[1:0]
BRIDGE
2304
MASTER RECEIVER
SLAVE RECEIVER
1
0
RX RDY
RX CLK
RX DATA
RX RSV
RX CNTRL[1:0]
BRIDGE

FIG. 23

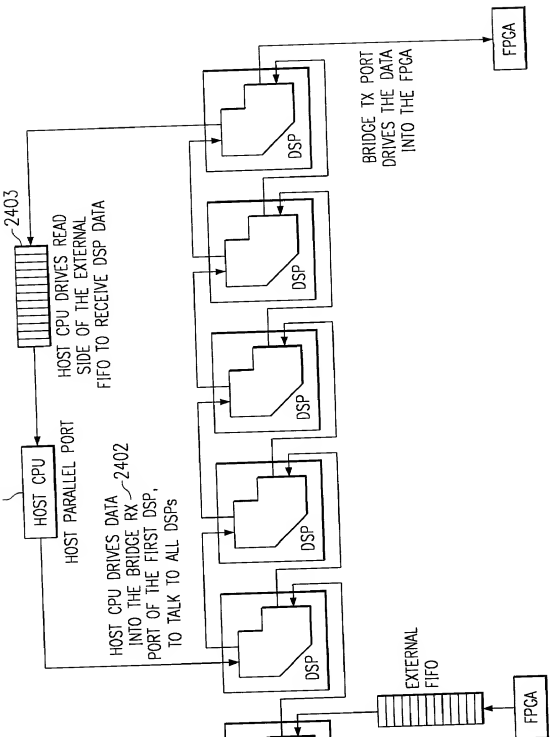

2401
HOST CPU
HOST PARALLEL PORT
2403
HOST CPU DRIVES READ SIDE OF THE EXTERNAL FIFO TO RECEIVE DSP DATA
HOST CPU DRIVES DATA INTO THE BRIDGE RX PORT OF THE FIRST DSP, TO TALK TO ALL DSPs
2402
DSP
DSP
DSP
DSP
DSP
BRIDGE TX PORT DRIVES THE DATA INTO THE FPGA
FPGA
EXTERNAL FIFO
FPGA
FPGA
THIS RX_PORT HAS TO BE INACTIVE IF THE OTHER RX_PORT IS RECEIVING PURE DATA FROM A FIFO
NORMALLY A SLAVE, THIS RX_PORT IS CONFIGURED AS A MASTER TO DRIVE THE DATA OUT OF THE FIFO

FIG. 24

DOCKET: 82650660

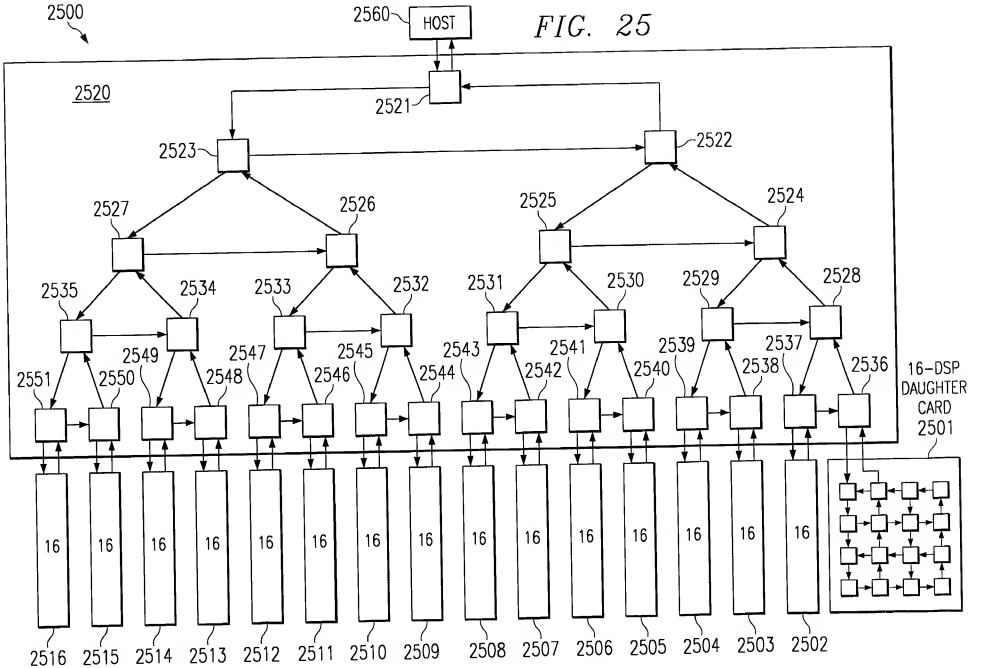


FIG. 25